

ATTACHMENT B**Amendments to the Specification**

Please replace paragraphs [0086] to [0089]] with the following amended paragraphs.

[0086] ~~When In Figure 4b, when~~ the logic function is a type AND logic function, each first 20 and second 21 logic cell includes an AND gate receiving the envelope logic signal E_j in one of their inputs and the symbol element $a(k)$, $b(k)$ respectively in the other of their inputs, in order to deliver the validated encoded symbol $S'(k)$ or the pause symbol $Sr(k)$.

[0087] ~~When In Figure 4c, when~~ the logic processing corresponds to a type OR logic function with the complemented envelope signal, the first 20 and the second 21 logic cells are formed by an OR gate receiving in one of their inputs the envelope logic signal E_j by means of an inverter, and in the other of their inputs, the symbol element $a(k)$, $b(k)$ in order to deliver the validated encoded symbol $S'(k)$ and the pause symbol $Sr(k)$.

[0088] ~~When In Figure 4d, when~~ the logic processing corresponds to a type AND logic function with the complemented envelope logic signal, the first 20 and the second 21 logic cell comprise an AND gate one of the inputs of which receives the envelope logic signal by means of an inverter and the other of the inputs receives the corresponding symbol element $a(k)$, $b(k)$ in order to deliver the validated encoded symbol $S'(k)$ or the pause symbol $Sr(k)$.

[0089] ~~When In Figure 4e, when~~ the logic processing corresponds to a type OR logic function between the symbol elements of the encoded symbols $a(k)$, $b(k)$ and envelope logic signal E_j the first 20 and the second 21 logic cell consist of a gate OR receiving, in one of their inputs the envelope logic signal E_j and in the other of their inputs, the symbol element $a(k)$, respectively $b(k)$ in order to deliver the validated encoded symbols $S'(k)$ or pause symbols $Sr(k)$.